VIDEO DISPLAY PROCESSOR

(V. D. P.)

TMS 3536

PRELIMINARY SPECIFICATION

THIS DOCUMENT CONTAINS
INFORMATION ON A NEW
PRODUCT; SPECIFICATIONS
ARE SUBJECT TO CHANGE
WITHOUT NOTICE

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SECTION 1 : GENERAL FEATURES

1.0 SCOPE

THIS SPECIFICATION ESTABLISHES THE FUNCTIONAL SPECIFICATION OF THE TMS 3536 VIDEO DISPLAY PROCESSOR (V.D.P.)

1.1 CHARACTERISTICS

THE VIDEO DISPLAY PROCESSOR (V.D.P.) IS DESIGNED TO PRODUCE SIGNALS REQUIRED FOR DISPLAY OF ALPHANUMERIC CHARACTERS, BLOCK GRAPHICS AND FIGURES DEFINED ON A DOT-BY-DOT BASIS ON A COLOR OR BLACK/WHITE TELEVISION OR MONITOR.

MODES OF OPERATION, DISPLAY AND ADDRESSING ARE DIRECTLY PROGRAMMABLE BY ON-CHIP COMMAND REGISTERS. CHARACTERISTICS OF DISPLAYED CHARACTERS, VIDEO CONTROL SIGNALS, ETC. ARE PROGRAMMABLE BY A SINGLE MASK LEVEL CHANGE.

ACCESS TO THE MEMORY ASSOCIATED WITH THE VDP IS CONTROLLED BY A SYSTEM OF TRANSPARENT ASYNCHRONOUS DIRECT MEMORY ACCESS (D.M.A.) ITS CAPACITY MAY BE EASILY ADAPTED TO ANY PARTICULAR APPLICATION : FROM THE MINIMUM SIZE REQUIRED FOR A SINGLE PAGE DISPLAY STORAGE TO MULTI-PAGE 64K BYTES BLOCKS. THE VDP PROVIDES AUTOMATIC REFRESH FOR DYNAMIC MEMORIES (DRAM)

ALL DATA TRANSFERS BETWEEN THE VDP, THE PROCESSING UNIT (MCU) AND THE ASSOCIATED MEMORY ARE IN BYTE FORM. THE PROCESSING UNIT MAY CONVENIENTLY USE 4; 8 OR 16-BIT MICROPROCESSORS.

THE VDP PROVIDES R, G, B INFORMATION AND A COMPOSITE SYNC SIGNAL TO THE DISPLAY SCREEN. THIS COMPOSITE SIGNAL ALLOWS GENERATION OF VIDEO-COMPOSITE INFORMATION. A FAST SWITCHING CONTROL SIGNAL IS ALSO PROVIDED TO ALLOW INSERTION (OR BOXING) OF TELETEXT INFORMATION INTO A NORMAL VIDEO PICTURE.

1.2 ARCHITECTURE

A TYPICAL ARCHITECTURE IS SHOWN IN FIGURE 1. THE VDP IS CONNECTED TO :

- THE PROCESSING UNIT (MCU)
- THE MEMORY BLOCK
- A TELETEXT DATA PROVIDER
- A TV INTERFACE

FOR ACQUISITION OF BROADCAST INFORMATION, THE DATA PROVIDER WILL RECEIVE THE VIDEO-COMPOSITE SIGNAL FROM THE TV INTERFACE STAGE AND MAY CONSIST OF THE SN 96533N DATA SLICER AND THE TMS 3534 A NL PREFIX PROCESSOR.

1.2.1 PROCESSING UNIT (MCU)

E1, E2, RWM AND RDY CONTROL SIGNALS ARE USED FOR DATA TRANSFERS BETWEEN THE MCU AND THE VDP ON THE 8-BIT MPU BUS (M0 TO M7). THESE CONTROL SIGNALS ALLOW ACCESS TO THE INTERNAL VDP REGISTERS AND TO THE MEMORY.

1.2.2 MEMORY BLOCK

RAS, CAS AND RW CONTROL SIGNALS ARE USED FOR ADDRESSES AND DATA TRANSFERS BETWEEN THE VDP AND THE MEMORY BLOCK ON THE 8-BIT DATA BUS (D0 TO D7). DYNAMIC OR STATIC MEMORY MAY BE USED. THE MEMORY PARTITIONING WILL USUALLY INCLUDE :

- ONE OR SEVERAL FIELDS USED AS BUFFERS FOR THE INFORMATION ISSUED BY THE DATA PROVIDER.
- ONE OR SEVERAL FIELDS USED AS PAGE DISPLAY MEMORIES.
- ONE OR SEVERAL FIELDS CONTAINING THE ALPHANUMERIC AND BLOCK-GRAPHIC CHARACTER GENERATORS.

THE SIZE AND LOCATION OF THESE FIELDS WITHIN THE MEMORY ARE FULLY PROGRAMMABLE BY THE PROCESSING UNIT.

1.2.3 DATA PROVIDER

HMP AND HIZ CONTROL SIGNALS ARE USED FOR DATA TRANSFER FROM THE DATA PROVIDER TO THE BUFFER MEMORY THROUGH THE DATA BUS. HMP IS A BYTE CLOCK AND HIZ A TRANSFER ENABLE SIGNAL.

1.2.4 TV INTERFACE

THE VDP IS CONNECTED TO THE TV INTERFACE BY THE FOLLOWING SIGNALS :

- R, G, B INFORMATION
- A FAST SWITCHING CONTROL SIGNAL I
- LINE SYNC (SLL) AND FRAME SYNC (SCT) INFORMATION
- LINE AND FRAME COMPOSITE CONTROL SIGNAL (SCM)

THE SCM COMPOSITE CONTROL MAY BE COMBINED WITH R, G, B DATA TO REGENERATE COMPOSITE VIDEO INFORMATION.

1.2.5 PROCESSING AND DISPLAY MODES OF OPERATION

THE PROCESSING UNIT PROGRAMS THE VDP OPERATION MODE, SPECIFIES A FIELD FOR THE BUFFER MEMORY AND ANOTHER FOR THE PAGE DISPLAY MEMORY AND LOADS THE CHARACTER GENERATORS INTO A FURTHER FIELD WHEN THE VIDEOTEX MODE OF OPERATION IS SELECTED (I.E. DISPLAY OF ALPHANUMERIC AND BLOCK-GRAPHIC CHARACTERS).

WHEN OPERATING IN THE VIDEOTEX MODE, CODED INFORMATION ISSUED BY THE DATA PROVIDER ARE LOADED INTO THE BUFFER MEMORY. THE MCU WILL THEN READ THIS INFORMATION THROUGH THE VDP AND DECODE AND GENERATE A 2 BYTE WORD FOR EACH CHARACTER TO BE DISPLAYED ON THE SCREEN. THIS 2 BYTE WORD WHICH INCLUDES THE CHARACTER CODE AND ITS ATTRIBUTES IS THEN DOWN-LOADED INTO THE PAGE DISPLAY MEMORY BY THE PROCESSING UNIT.

DURING THE PERIOD OF TIME ALLOCATED TO SCREEN DISPLAY THE VDP WILL PERIODICALLY ACCESS THE CHARACTER CODE AND ATTRIBUTES OF THE CHARACTERS TO BE DISPLAYED. IT WILL ALSO ACCESS THE CHARACTER MATRIX PATTERN, DEFINED BY THE CHARACTER CODE CONTAINED IN THE SELECTED CHARACTER GENERATOR. THE VDP WILL THEN DEFINE THE R, G AND B INFORMATION ACCORDING TO THE DISPLAY ATTRIBUTS FOR EACH DOT OF THE SCREEN.

WHEN OPERATING IN MAPPING MODE, THE PROCESSING UNIT LOADS THE COLOR INFORMATION FOR EACH DOT DIRECTLY INTO THE PAGE DISPLAY MEMORY.

DURING THE PERIOD OF TIME ALLOCATED TO SCREEN DISPLAY THE VDP PERIODICALLY READS THE DOT COLOR INFORMATION OUT OF THE MEMORY.

1.3 INTERNAL ARCHITECTURE OF THE VIDO DISPLAY PROCESSOR

THE VDP PERFORMS 3 FUNCTIONS, EACH CORRESPONDING TO AN INDIVIDUAL BLOCK (FIG. 2) :

- CONTROL UNIT
- TIME BASE
- DECODER

THE CONTROL UNIT MONITORS INFORMATION EXCHANGES BETWEEN THE MCU, THE MEMORY, THE DATA PROVIDER AND THE VDP ITSELF.

THE TIME BASE ESSENTIALLY PROVIDES DISPLAY SYNCHRONISATION.

THE DECODER, FROM THE PAGE DISPLAY MEMORY CONTENTS, GENERATES SERIAL DOT COLOR INFORMATION.

SECTION II: FUNCTIONAL SPECIFICATION

2.1 THE CONTROL UNIT (FIG.3)

THE CONTROL UNIT CONTAINS A 16 BIT ARITHMETIC LOGIC UNIT (ALU) AND A MEMORY CONSISTING OF ACCUMULATION REGISTERS AND BASE ADDRESS REGISTERS. THE ALU COMPUTES ALL MEMORY ACCESS ADDRESSES AND CONTROLS THE SIZE OF INDIVIDUAL MEMORY FIELDS.

THE VDP OPERATING MODE IS PROGRAMMED INTO THE COMMAND REGISTERS BY THE PROCESSING UNIT.

AN 8-BIT STATUS REGISTER ALLOWS THE PROCESSING UNIT TO KEEP TRACK OF THE VDP INTERNAL STATE.

THE DMA CONTROLLER MONITORS ALL DATA EXCHANGES BETWEEN THE MEMORY AND:

- THE PROCESSING UNIT
- THE DATA PROVIDER
- THE VDP DECODER

EACH CHANNEL OF TRANSFER IS TRANSPARENT TO THE 2 OTHER CHANNELS : THE DATA PROVIDER MAY ACCESS THE BUFFER MEMORY WITHOUT INTERRUPTING OR SLOWING DOWN THE PROCESSING UNIT AND THE DECODER MAY ACCESS TO THE PAGE DISPLAY MEMORY WITHOUT INTERRUPTING OR SLOWING DOWN THE 2 OTHER CHANNELS.

THE ADDRESSES PROVIDED BY THE ALU GIVE ACCESS TO THE VARIOUS BUFFERS, PAGE MEMORIES AND CHARACTER GENERATORS. THE MCU ALSO USES THIS ADDRESSING PROCESS. DATA WILL BE TRANSFERRED BETWEEN THE DATA BUS AND THE CPU BUS THROUGH THE DATA REGISTER.

WHEN OPERATING IN VIDEOTEX MODE, THE DISPLAY REGISTERS CONTAIN THE LATEST CHARACTER CODE AND ATTRIBUTES READ OUT OF THE PAGE DISPLAY MEMORY AND THE 8 DOTS OF THE CHARACTER TO BE DISPLAYED PROVIDED BY THE CHARACTER GENERATOR. IN MAPPING MODE, THESE REGISTERS CONTAIN THE COLOR OF THE 8 DOTS TO BE DISPLAYED.

2.1.1 COMMAND REGISTERS OPERATION

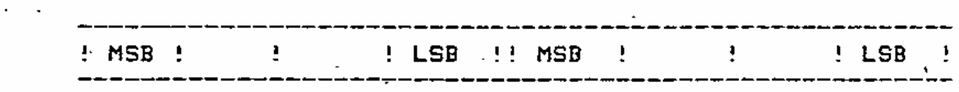
THE COMMAND REGISTERS BLOCK CONSISTS OF :

- E1, E2 AND RWN DECODE LOGIC
- A POINTER FOR COMMAND REGISTERS, STATUS REGISTER AND BASE ADDRESS REGISTER ACCESS
- COMMAND AND STATUS REGISTERS

THE FUNCTION OF THE E1 ET E2 INPUT SIGNALS IS DESCRIBED IN TABLE 1. THE E1 = E2 = 1 COMBINATION CORRESPONDS TO AN INACTIVE STATE. THE E1 AND E2 INPUTS MUST RETURN TO THE INACTIVE STATE BEFORE A NEW ACCESS IS REQUESTED. THE E1 = 0, E2 = 1 COMBINATION ALSO MODIFIES THE POINTER STATE.

THE POINTER IS LOADED WHILE IN THE ZERO STATE. IT CONTAINS 2 ADDRESS FIELDS OF 4 BITS EACH WHICH ARE :

- REGISTER ACCESS ADDRESS (TABLE 2)
- RETURN ADDRESS (AFTER ACCESS)



THE POINTER WILL RETURN TO THE ZERO STATE EITHER WHEN E2 = 0 OR WHEN THE RETURN ADDRESS IS ZERO.

2.1.2 POINTER OPERATION

AFTER A MEMORY ACCESS CYCLE (E2=0), THE POINTER RETURNS TO ZERO.

DURING THE NEXT MCU ACCESS TO THE VDP, THE M0-M7 BUS CONTENT IS LOADED INTO THE POINTER REGISTER.

DURING THE FOLLOWING ACCESS TO THE VDP, THE M0-M7 BUS CONTENT IS LOADED INTO THE REGISTER ADDRESSED BY THE POINTER CONTENTS.

IF THE RETURN ADDRESS IS ZERO, A NEW ADDRESS MAY BE LOADED INTO THE POINTER AT THE NEXT VDP ACCESS. IF THE RETURN ADDRESS IS NOT ZERO, THE M0-M7 BUS CONTENT IS LOADED INTO A DIFFERENT REGISTER THE ADDRESS OF WHICH IS EQUAL TO THE RETURN ADDRESS FIELD CONTENT. IN THIS CASE, ONLY A MEMORY ACCESS (E2=0) CAN RESET THE POINTER TO ZERO.

2.1.3 REGISTERS CONTENT ASSIGNMENT

- ROW AND COL REGISTERS

THESE 2 REGISTERS ARE LOADED BY THE PROCESSING UNIT AT THE POINTER ADDRESS VALUE 1 FOR COL AND VALUE 2 FOR ROW.

THE LOADING OF ONE OF THE BASE ADDRESSES BETWEEN BAMT AND BAMTF TRANSFERS THE COL AND ROW REGISTER CONTENTS INTO THE SELECTED BASE ADDRESS.

- STATUS REGISTER

THE STATUS REGISTER CONTAINS THE VDP STATE. THE MCU CAN ONLY READ THE CONTENT OF THIS REGISTER WHICH IS VALIDATED ON TO THE M0-M7 BUS AFTER A CYCLE COMPLETION.

THE MEANING OF THE ST1 TO ST8 BITS IS SPECIFIED BY TABLE 3. THE ST2 BIT RECEIVES THE FRAME SYNC SIGNAL ISSUED BY THE TIME BASE. THIS SIGNAL IS SYNCHRONIZED WITH THE FRAME SYNC OF THE NORMAL TV VIDEO. ST2 = 1 DURING THE FRAME SYNC PULSE. ST4 = 1 MEANS THAT AN ERROR HAS OCCURED DURING THE LAST MCU MEMORY READ CYCLE. ST4 IS UP-DATED AT EACH MCU MEMORY READ CYCLE.

ST5 = 1 MEANS THAT THE PROCESSING UNIT MAY ACCESS THE MEMORY. THIS INFORMATION IS PROVIDED BY THE DMA CONTROLLER BLOCK.

ST7 AND ST8 ARE USED BY THE LOGIC ASSOCIATED WITH THE BUFFER MEMORY (REFER TO PARAGRAPH 2.1.1.5).

- CM1 REGISTER

REFER TO PARAGRAPH 2.2.
NOTE :
THE LOADING OF THE CM1 REGISTER SETS THE VDP INITIALIZATION FLIP-FLOP, WHICH IS RESET AS SOON AS A BASE ADDRESS IS STORED IN THE VDP. THE VDP ACTIVATION MUST START WITH A CM1 REGISTER LOADING AND ANY CM1 ACCESS MUST BE FOLLOWED BY THE LOADING OF A BASE ADDRESS. DURING THE INI-TIALISATION (BETWEEN CM1 LOADING AND A BASE ADDRESS LOADING) DISPLAY ON THE TV SCREEN IS INHIBITED.

- CM2 REGISTER

REFER TO PARAGRAPH 2.3.

- CM3 REGISTER (TABLE 4.1)

CT1 AND CT2 ALLOW SELECTION OF 3 MODES OF DISPLAY :

* IN MAPPING MODE THE COLOR ASSOCIATED WITH EACH SCREEN DOT IS DIRECT-LY DEFINED BY THE PROCESSING UNIT.

* IN VIDEOTEX MODE, THE ALPHANUMERIC AND BLOCK-GRAPHIC CHARACTERS BEING STORED IN THE CHARACTER GENERATORS, THE PROCESSING UNIT DEFINES THE ATTRIBUTES AND CHARACTER CODE OF EACH CHARACTER.

* IN MIX MODE, THE TWO ABOVE MENTIONED MODES MAY BE USED WITHIN THE SAME PAGE. A GIVEN LINE OR ROW MUST ALWAYS BE EITHER IN PURE VIDEOTEX OR MAPPING MODE.

WHEN CT1 = CT2 = 0, THE DISPLAY AS WELL AS THE MEMORY ACCESS ARE IN-HIBITED. R,G, AND B OUTPUTS ARE HELD AT ZERO

WHEN CT4 = 1, MCU MEMORY ACCESS REQUESTS ARE INHIBITED DURING THE PAGE DISPLAY (ABOUT 50 % OF THE FRAME SCANNING DURATION) THUS LEAVING MORE TIME FOR VDP DECODER AND DATA PROVIDER ACCESS TO THE MEMORY WHICH, IN TURN, MAY USE COMPONENTS WITH RELAXED MINIMUM CYCLE TIME DURATIONS. THE PROCESSING UNIT KNOWS WHEN IT MAY ACCESS TO THE MEMORY BY TESTING THE ST5 BIT OF THE STATUS REGISTER.

CT5 ALLOWS SELECTION OF ONE OUT OF TWO TIMING DIAGRAMS FOR RAS AND CAS. THESE TIMING DIAGRAMS MAY ALSO BE MODIFIED BY A MASK CHANGE OR ADJUSTED BY TRIMMING OF THE EXTERNAL COMPONENTS TIED TO THE ODE AND ODS INPUT/OUTPUT LINES.

TABLE 4.2 GIVES THE ADDRESSING FIELD ASSIGNMENT USED FOR SEVERAL TYPES OF MEMORIES.

- BASE ADDRESS REGISTERS

THE CONTENTS OF REGISTERS BAMT TO BAMTF (ADDRESSES 8 TO F OF THE POINTER) REPRESENT THE BASE ADDRESSES FOR THE VARIOUS FIELDS WITHIN THE MEMORY. EACH BASE ADDRESS USES 16 BITS. LOADING OF THESE BASE ADDRESSES IS ACCOMPLISHED THROUGH THE COL AND ROW REGISTERS WHICH ARE DIRECTLY ACCESSIBLE BY THE MCU.

WHEN LOADED IN THE VDP, THE CHARACTER GENERATOR BASE ADDRESSES (BAGCO, 1, 2, AND 3 REGISTERS) ARE INCREMENTED BY 2, THE OTHER BASE ADDRESSES BY 1 ONLY.

THE BAMT AND BAMTF REGISTERS RESPECTIVELY DEFINE THE FIRST ADDRESS OF THE BUFFER MEMORY AND THE FIRST ADDRESS IMMEDIATELY FOLLOWING THE END OF THIS BUFFER. THE BUFFER MEMORY MAY BE LOCATED ANYWHERE WITHIN THE TOTAL MEMORY ARRAY AND ITS SIZE MAY TAKE ANY VALUE BETWEEN 1 BYTE AND 64 K BYTES.

SEVERAL BUFFER MEMORIES MAY EXIST WITHIN THE SAME MEMORY ARRAY BUT ONLY ONE IS USED AT A TIME BY THE MCU. BUFFER ADDRESSES AT WHICH INFORMATIONS ISSUED BY THE DATA PROVIDER WILL BE LOADED ARE COMPUTED BY THE ALU AND TRANSFERRED TO THE DATA BUS BY THE ADDRESS REGISTER. UPON UP-DATING OF THE BAMT AND BAMTF REGISTERS, THE BASE ADDRESSES ARE TRANSFERRED TO THE CORRESPONDING ACCUMULATOR AT THE NEXT DATA PROVIDER ACCESS. EACH SUBSEQUENT DATA PROVIDER ACCESS WILL INCREMENT THE CONTENT OF THE ADDRESS REGISTER.

THE BAMP REGISTER CONTAINS THE BASE ADDRESS FOR THE MEMORY FIELD ALLOCATED TO THE PROCESSING UNIT. ACCESS ADDRESSES ARE DIRECTLY INCREMENTED BY THE ALU. THE PROCESSING UNIT MAY DEFINE A SECOND WORK SPACE BY USING THE COL AND ROW REGISTERS THE CONTENTS OF WHICH ARE TRANSFERRED TO AN INTERNAL ACCUMULATOR UPON THE FIRST ACCESS FOLLOWING THE LOADING OF EITHER OF THESE 2 REGISTERS.

THE BAPA REGISTER CONTAINS THE BASE ADDRESS OF THE PAGE BEING DISPLAYED. ONLY ONE PAGE MEMORY MAY BE SELECTED AT A TIME. HOWEVER, THE MEMORY MAY STORE AS MANY PAGES READY FOR DISPLAY AS ITS SIZE AND PARTITIONING ALLOW. THE SIZE OF A PARTICULAR PAGE DISPLAY MEMORY WILL DEPEND ON THE TYPE OF DISPLAY BEING USED . IN VIDEOTEX MODE ITS SIZE DEPENDS ON THE NUMBER OF ROWS AND OF CHARACTERS PER ROW PROGRAMMED IN THE TIME BASE. IN MAPPING MODE, THE SIZE DEPENDS ON THE NUMBER OF LINES AND OF DOTS PER LINE WHICH HAVE BEEN DEFINED. IN MIX MODE, THE SIZE WILL DEPEND ON A COMBINATION OF THE ABOVE MENTIONED PARAMETERS. WHEN READING INFORMATION OUT OF THE PAGE DISPLAY MEMORY, THE ASSOCIATED ADDRESSES ARE COMPUTED BY THE ALU. WHILE SCANNING THE SCREEN, THE BAPA CONTENT IS TRANSFERRED TO THE DISPLAY ACCUMULATOR AT THE BEGINNING OF THE FIRST ROW. THE FIRST DISPLAYED CHARACTER MAKES USE OF THE BASE ADDRESS. THE ADDRESS IS THEN INCREMENTED FOR EACH SUBSEQUENT CHARACTER READ OUT OF THE PAGE DISPLAY MEMORY.

THE BASE ADDRESS BAPA MUST BE AN EVEN NUMBER AFTER BEING LOADED INTO THE VDP IN ORDER TO OBTAIN A CORRECT ADDRESSING DURING THE DOUBLE ACCESSES TO THE DISPLAY MEMORY.

BAGC00 TO BAGC3 REGISTERS CONTAIN THE BASE ADDRESSES OF 4 CHARACTER OR BLOCK GRAPHIC GENERATORS WHICH MAY BE USED IN VIDEOTEX OR MIX MODES. THE MEMORY MAY CONTAIN AS MANY CHARACTER OR BLOCK-GRAPHIC GENERATORS AS ALLOWED BY ITS SIZE AND PARTITIONING BUT ONLY 4 OF THEM MAY BE USED AT A TIME FOR A PARTICULAR PAGE DISPLAY. THE ADDRESS OF THE CHARACTER MATRIX IS DEFINED BY THE ALU BY ADDING THE 16 BITS OF THE BASE ADDRESS TO THE CHARACTER CODE AND TO THE NUMBER OF THE CURRENT LINE OF THE MATRIX BEING DISPLAYED. EACH CHARACTER ATTRIBUTE SELECTS ONE CHARACTER GENERATOR OUT OF 4. IN MAPPING MODE, THE CHARACTER GENERATORS ARE NOT USED.

2.1.4 DMA FUNCTIONAL DESCRIPTION

- THE ASYNCHRONOUS TRANSPARENT DMA SYSTEM ALLOWS ACCESS TO A COMMON EXTERNAL MEMORY THROUGH THREE SEPARATE CHANNELS.

- MEMORY ACCESS THROUGH ONE CHANNEL DOES NOT DISTURB NOR SLOW DOWN ANY OTHER ACCESS TAKING PLACE ON EITHER OF THE OTHER 2 CHANNELS. THIS FEATURE ALLOWS THE FOLLOWING OPERATIONS TO TAKE PLACE SIMULTANEOUSLY:

  . DISPLAY OF ONE PAGE ON THE TV SCREEN
  . DATA PROCESSING BY THE PROCESSING UNIT
  . DATA LOADING BY THE DATA PROVIDER

- EACH CHANNEL IS ASSOCIATED WITH ONLY ONE TYPE OF ACCESS :

  . DATA PROVIDER
  . PROCESSING UNIT
  . DISPLAY

- THE ACCESS REQUESTED FROM THE VARIOUS SOURCES ARE STORED IN THE DMA THEN EXECUTED ACCORDING TO THE FOLLOWING PRIORITY RANKING :

1. DATA PROVIDER
2. PROCESSING UNIT
3. DISPLAY

DURING THE EXECUTION OF EACH ACCESS THE CIRCUITRY GENERATES THE APPROPRIATE CONTROL SIGNALS TO THE MEMORY : RAS, CAS, AND R/W. THE TIMING OF THESE SIGNALS IS STORED IN A MASK PROGRAMMABLE ROM AND ONE OUT OF TWO TYPES OF TIMING CAN BE SELECTED BY THE COMMAND BIT CT5. FREQUENCY ADJUSTMENT IS ALSO MADE POSSIBLE BY THE MEANS OF PINS ODE AND ODS WHICH, TOGETHER WITH TIMING SELECTION, ALLOW COMPATIBILITY WITH MOST MEMORIES AVAILABLE ON THE MARKET.

2.1.5 AUTO-INCREMENT ADDRESSING MECHANISM

- TWO ACCUMULATORS ACMP AND ACMPXY TOGETHER WITH THE ADDER ARE USED BY THE PROCESSING UNIT FOR THE AUTO-INCREMENT ADDRESSING.

- THE ACMP ACCUMULATOR IS LOADED WITH THE BASE ADDRESS BAMP, AND THE ACMPXY ACCUMULATOR IS LOADED WITH THE CONTENTS OF TWO REGISTERS COL AND ROW DURING THE FIRST MEMORY ACCESS FOLLOWING THE LOADING OF ONE OF THESE TWO REGISTERS.

- THE ADDRESS TRANSFER INTO ACMPXY SETS THE INCREMENTATION MODE. IF THE FIRST MEMORY ACCESS AFTER THE TRANSFER IS A WRITE CYCLE THEN ALL THE FOLLOWING WRITE CYCLES WILL USE THE ACMPXY ACCUMULATOR AND EACH ACCESS WILL INCREMENT BY 1 THE CONTENT OF ACMPXY. THE READ CYCLES WILL THEN USE THE ACMP ACCUMULATOR AND EACH READ ACCESS WILL INCREMENT BY 1 THE CONTENT OF ACMP. THIS MECHANISM WORKS THE OTHER WAY AROUND IF THE FIRST ACCESS IS A READ CYCLE AFTER THE ADDRESS TRANSFER INTO ACMPXY. THE SAME FUNCTION ALSO APPLIES WHEN REPLACING ACMPXY BY ACMP.

- THE CONTENT OF THE TWO REGISTERS COL AND ROW IS TRANSFERRED INTO THE BASE ADDRESS REGISTER BAMP WHEN THE POINTER INDICATES ADDRESS "9".

- NOTE THAT ONLY THE TRANSFER OF COL AND ROW IN ACMPXY OR BAMP MAY MODIFY THE AUTOINCREMENT ADDRESSING MODE, ANY OTHER TRANSFER OF COL AND ROW LEAVE IT UNCHANGED.

THE 16 BITS OF THE BASE ADDRESS BAMP ARE TRANSFERRED INTO THE ACCUMULATOR ACMP DURING THE FIRST CYCLE ALLOCATED TO IT, THAT IS AT THE FIRST READ CYCLE FOLLOWING COL AND ROW TRANSFER INTO BAMP FOR THE EXAMPLE MENTIONED IN THE PREVIOUS PARAGRAPH. THE CONTENT OF BAMP IS ALSO TRANSFERRED IN THE ACMP REGISTER, WHEN THE CONTENTS OF THE ING REGISTERS ACMP AND BAMTF ARE EQUAL.

THIS MECHANISM CAUSES THE ADDRESS TO INCREMENT BETWEEN TWO BOUNDARIES BAMP AND BAMTF AND THUS DEFINES THE ASSOCIATED MEMORY FIELD.

- FIGURE 4 INDICATES TWO TYPES OF TIMING DIAGRAM.

- IN ORDER TO PERFORM A MEMORY ACCESS, TWO TYPES OF MEMORY CYCLES ARE GENERATED BY THE VDP :

  . SINGLE ACCESS CYCLE : READ OR WRITE ONE BYTE (8BITS) TO OR FROM MEMORY. THIS TYPE OF CYCLE IS USED DURING THE ACCESS BY THE MPU, THE DATA PROVIDER AND ACCESS TO ONE OF THE CHARACTER GENERATORS.

  . DOUBLE ACCESS CYCLE : READ OR WRITE TWO ADJACENT BYTES TO OR FROM MEMORY. USED TO READ THE CHARACTER CODE AND THE ATTRIBUTES FROM THE PAGE MEMORY.

- DURING A MEMORY ACCESS, THE SAME BUS IS USED TO TRANSMIT ROW AND COLUMN ADDRESSES (2 BYTES) AS WELL AS THE DATA.

- THE ROW ADDRESS IS VALID DURING RAS FALLING EDGE (1 - FIGURE 4); AND THE COLUMN ADDRESS DURING CAS FALLING EDGE (2). DURING A READ CYCLE, THE DATA BYTE IS AVAILABLE ON THE BUS AT THE END OF THE CYCLE (3); DURING A WRITE CYCLE (4), THE DATA BYTE IS VALID DURING THE R/W SIGNAL.

2.1.6 BUFFER MEMORY CONTROL

- THE BUFFER MEMORY STORES THE DATA INCOMING FROM THE DATA PROVIDER, THIS DATA IS THEN TRANSCODED BY THE MPU WHICH WRITES THE PAGE TO BE DISPLAYED INTO THE PAGE MEMORY.

- THE BUFFER MEMORY SIZE IS DEFINED BY THE CONTENT OF THE TWO REGISTERS BAMT AND BAMTF. BAMT CONTAINS THE FIRST ADDRESS OF THE MEMORY FIELD AND BAMTF CONTAINS THE FIRST ADDRESS OF THE NEXT MEMORY FIELD. THE ACTION OF STORING A BYTE INTO THE BUFFER MEMORY FROM THE DATA PROVIDER INCREMENTS THE CONTENTS OF ACMT.

- THE ACCUMULATOR ACMP IS INCREMENTED WHENEVER THE PROCESSING UNIT READS A BYTE FROM THE BUFFER MEMORY.

- WHEN THE CONTENTS OF ACMT AND ACMP ARE EQUAL, THE STATUS BIT ST8 OF THE STATUS REGISTER IS SET TO LOGICAL 1, INDICATING THAT THE PROCESSING UNIT HAS READ ALL THE BYTES CONTAINED IN THE BUFFER MEMORY

- IF ACMT (OR ACMP) IS FOUND EQUAL TO BAMTF THE BASE ADDRESS STORED IN BAMT (OR BAMP) IS TRANSFERRED TO ACMT (OR ACMP)

- WHENEVER THE CONTENTS OF ACMT AND ACMP ARE FOUND EQUAL WHILE THE DATA PROVIDER IS ONE BUFFER MEMORY AHEAD OF THE PROCESSING UNIT : OVERFLOW IS DETECTED AND THE STATUS BIT ST7 IS SET TO LOGICAL 1. DATA LOADING INTO THE BUFFER MEMORY FROM THE DATA PROVIDER IS THEN INTERRUPTED, NEVERTHELESS THE DATA STORED CQN BE RETRIEVED BY THE PROCESSING UNIT.

- ONCE THE OVERFLOW OF THE BUFFER MEMORY HAS BEEN DETECTED, THE DATA PROVIDER MUST BE RESET AND THE BASE ADDRESSES BAMT AND BAMTF RELOADED. INTO THE VDP.

ACMP → lecture
charge aussi BAMP.
ACMPXY → écriture.
charge aussi le 1er accès.

THE BUFFER MEMORY SIZE IS PROGRAMMED BY CHANGING ITS BOUNDARIES, (BAMT, BAMTF) AND THUS, MAY BE ADJUSTED TO THE DATA INPUT RATE AND THE PROCESSING SPEED.

2.1.7 CHARACTER GENERATORS LOADING (FIGURE 5)

- THE CHARACTER GENERATORS ARE USED IN VIDEOTEX MODE OR MIX MODE; 4 GENERATORS MAY BE USED FOR THE SAME PAGE. THEIR LOCATION WITHIN THE MEMORY IS DEFINED BY THE CONTENTS OF THE FOLLOWING 4 BASE ADDRESS REGISTERS : BAGC0, BAGC1, BAGC2 AND BAGC3. EACH GENERATOR CONTAINS 128 CHARACTERS OR BLOCK-GRAPHICS. THE CHARACTER CODES AND THE ATTRIBUTES (ALPHABET CODES) OF THE DISPLAY PAGE MEMORY MAY ADDRESS ANY ONE OF THESE CHARACTERS OR BLOCK-GRAPHICS.
- EACH CHARACTER IS DEFINED BY AN 8 DOT BY N LINE MATRIX, N BEING FIXED BY THE TIME BASE PROGRAMMATION; AN 8 DOT BY 10 LINE MATRIX IS PROGRAMMED IN THE STANDARD VERSION. THE BYTE DEFINING THE LAST LINE OF THE 1ST CHARACTER IS STORED AT THE BASE ADDRESS BAGC (N) AND THOSE DEFINING THE LAST LINES OF THE 127 REMAINING CHARACTERS ARE STORED AT THE FOLLOWING ADDRESSES. THE LAST BYTE OF ONE CHARACTER GENERATOR CONTAINS THE 1ST LINE OF THE 128TH CHARACTER. EACH CHARACTER GENERATOR STORES 1280 BYTES (10 BYTES X 128 CHARACTERS).

- THE CHARACTER GENERATORS MAY BE SEPARATED FROM ONE ANOTHER OR BE CONTIGUOUS WITHIN THE MEMORY.

  THEY CAN BE IMPLEMENTED AS RAM IN WHICH CASE THE CONTENTS MUST BE LOADED BY THE PROCESSING UNIT, THEY MAY ALSO BE IMPLEMENTED AS ROM INCLUDED IN THE MEMORY ASSOCIATED TO THE VDP.

- EACH PAGE DISPLAY MEMORY MAY INVOLVE SEPARATE CHARACTER GENERATORS OR SHARE A PART OF THE SAME GENERATOR.

2.1.8 LOADING OF THE PAGE DISPLAY MEMORY

- THE MEMORY ASSOCIATED TO THE VDP MAY INCLUDE SEVERAL MEMORY FIELDS ALLOCATED TO DIFFERENT PAGES TO BE DISPLAYED. EACH PAGE CAN BE COMPOSED USING VIDEOTEX, BLOCK-GRAPHIC, OR MIX MODE. ONLY ONE PAGE CAN BE DISPLAYED AT A TIME, DEFINED BY ITS BASE ADDRESS BAPA, ITS CHARACTER GENERATORS BAGC (N) AND BY ITS MODE OF OPERATION DECODED FROM BITS CT1 AND CT2.

VIDEOTEX MODE

- IN THIS OPERATION MODE THE PAGE MEMORY STORES THE CHARACTER CODES AND THE ATTRIBUTES OF EACH CHARACTER TO BE DISPLAYED. THE NUMBER OF ROWS AND THE NUMBER OF CHARACTERS ON EACH ROW IS GENERATED BY THE TIME BASE. THE LOADING OF THE PAGE MEMORY IS DESCRIBED BELOW FOR 25 ROWS OF 40 CHARACTERS EACH.

- THE BIT DISTRIBUTION OF THE TWO BYTES DEFINING ONE CHARACTER IS INDICATED IN FIG. 6, AND THE FUNCTION OF EACH OF THESE BITS IS EXPLAINED IN THE DECODER DESCRIPTION. THE MOST SIGNIFICANT BYTE OF THE FIRST CHARACTER TO BE DISPLAYED IS STORED AT THE BASE ADDRESS BAPA (FIG. 7), THE LEAST SIGNIFICANT BYTE OF THIS FIRST CHARACTER IS STORED AT THE NEXT ADDRESS. ATTRIBUES AND CHARACTER CODES OF THE 25 ROWS OF 40 CHARACTERS ARE STORED IN SERIES, NEXT TO ONE ANOTHER IN THE PAGE MEMORY. ONE 40 CHARACTER ROW CONTAINS 80 BYTES AND ONE 25 ROW PAGE CONTAINS 2000 BYTES.

MAPPING MODE (DOT BY DOT)

- IN THIS MODE OF OPERATION, THE PAGE DISPLAY MEMORY STORES THE COLOR INFORMATION FOR EACH DOT OF THE PAGE. EACH DOT IS DEFINED BY 3 BITS : R, G AND B; 3 BYTES ARE THEN NECESSARY TO DEFINE 8 DOTS. FOR A TIME-BASE PROGRAMMED WITH 25 ROWS OF 40 CHARACTERS, EACH LINE CONTAINS 320 DOTS (8x40), THE PICTURE IS THEN COMPOSED OF 250 LINES (25x10) AND INCLUDES 80 000 DOTS.

- EACH LINE OF DOTS IS DEFINED BY 40 GROUPS OF 3 BYTES, THE FUNCTION OF EACH BIT FOR EACH GROUP IS INDICATED IN FIG. 8.

- ONE BYTE CORRESPONDS TO ONE COLOR. THE FIRST BYTE IS LOCATED AT THE BASE ADDRESS BAPA AND CONTAINS BITS B1 THROUGH B8 OF THE FIRST 8 DOTS OF THE PICTURE, THE SECOND BYTE CONTAINS BITS G1 THROUGH G8 AND THE THIRD BYTE, BITS R1 THROUGH R8. THE M.S.B. OF EACH OF THE 3 FIRST BYTES DEFINE THE COLOR OF THE FIRST DOT OF THE PICTURE. THE FOLLOWING DOTS OF THE LINE ARE LOADED IN THE MEMORY UP TO ADDRESS BAPA + 119.

- THE NEXT BYTE (BAPA + 120) IS NOT DISPLAYED AND CONTAINS THE ATTRIBUTES ASSIGNED TO THE NEXT LINE. THE BYTE PLACED IN BAPA + 121 IS NECESSARY TO START THE NEXT LINE WITH AN EVEN ADDRESS AND ITS CONTENTS INDICATE THE POSITION OF AN ANALOG PICTURE INSERTION WINDOW WITHIN THE MAPPING PICTURE, ONE BIT CORRESPONDING TO A 40 DOT WINDOW.

- THE 250 LINES OF THE PICTURE ARE ORGANISED IN THE SAME MANNER.

- THE COLOR OF THE BORDER CAN BE MODIFIED AT EACH LINE.

MIX MODE

- FOR THIS MODE OF OPERATION, THE PAGE MEMORY STORES ROWS OF CHARACTERS OR BLOCK-GRAPHICS OBTAINED FROM A CHARACTER GENERATOR AS WELL AS LINES DEFINED DOT BY DOT. THE PAGE TO BE DISPLAYED CAN BE ANY ARRANGEMENT OF VIDEOTEX ROWS AND MAPPED LINES, THE ONLY RESTRICTION BEING THAT THE TOP ROW OF THE PICTURE MUST BE IN VIDEOTEX MODE.

- FOR A TIME BASE PROGRAMMED WITH 25 ROWS OF 40 CHARACTERS EACH, EACH VIDEOTEX ROW USES 80 BYTES FOR THE DISPLAY PLUS 2 BYTES FOR THE MODE OF OPERATION AND THE BORDER-COLOR FOR THE NEXT LINE OR ROW.

- ONE MAPPING LINE USES 120 BYTES FOR THE DISPLAY PLUS 2 BYTES FOR THE MODE OF OPERATION AND THE ATTRIBUTES OF THE NEXT LINE OR ROW. CONSEQUENTLY THE SIZE OF A MIX MODE PAGE MEMORY DEPENDS ON ITS ARRANGEMENT; IT MAY VARY FROM 2050 TO 29362 BYTES.

- AN EXAMPLE OF A MIX MODE MEMORY ORGANISATION IS SHOWN IN FIG. 10. IT IS MANDATORY FOR THE FIRST ROW TO BE A VIDEOTEX ROW. THE ATTRIBUTES AND CHARACTER CODE OF THE FIRST CHARACTER ARE LOCATED AT THE ADDRESS CONTAINED IN BAPA AND BAPA+1. THE COLOR OF THE BORDER OF THE NEXT ROW IS GIVEN BY THE BITS B, G, AND R WHICH ARE THE MSB'S OF THE BYTE BAPA+80.

  THE BIT "CG" SELECTS THE MODE OF OPERATION FOR THE NEXT LINE OR ROW :
  - . VIDEOTEX MODE : CG = 0
  - . MAPPING MODE : CG = 1

  ON FIG. 10 THE SECOND LINE IS A MAPPING LINE : CG = 1, IT INCLUDES 120 BYTES FOR THE DISPLAY. THE 121ST BYTE LOCATED AT ADDRESS BAPA+202 INDICATES THE BORDER-COLOR AS WELL AS THE MODE OF OPERATION OF THE NEXT ROW : CG = 0, THAT IS VIDEOTEX MODE.

- THE PLACEMENT OF ANY NUMBER OF MAPPING LINES BETWEEN TWO VIDEOTEX ROWS ALLOWS THE OPTIMISATION OF THE PAGE MEMORY SIZE BY KEEPING THE MAPPING MODE TO THE MINIMUM REQUIRED BY THE PICTURE TO BE IMPLEMENTED.

2.1.9 MEMORY-FIELD ORGANIZATIONS

- ONE EXAMPLE OF MEMORY ORGANIZATION IS SHOWN IN FIG. 11.

- EACH MEMORY FIELD POSITION IS DEFINED BY A 16 BIT BASE ADDRESS.

- THE MEMORY FIELDS ARE NOT FIXED NOR RESTRICTED TO ANY PARTICULAR FUNCTION. CONSEQUENTLY A 2K BYTE MEMORY (2048 BYTES) CAN BE PARTITIONED IN ONE PAGE DISPLAY MEMORY OF 25 ROWS OF 40 CHARACTERS AND ONE BUFFER MEMORY OF 48 BYTES. IN THE CASE WHERE THE PAGE HAS ONLY 21 ROWS THE BUFFER MEMORY CAPACITY CAN BE INCREASED TO 368 BYTES. A ROM IS THEN USED TO STORE THE CHARACTER GENERATOR.

2.2. TIME BASE (FIG.12)

- THE TIME BASE OF THE VDP CONTROLS AND CLOCKS THE DISPLAY OF INFORMATION ON THE TV SCREEN.

  IT IS COMPOSED OF :

  . AN INDUCTANCE OSCILLATOR PROVIDING THE DOT FREQUENCY
  . THREE MAIN COUNTERS : CHARACTER, LINE AND FRAME COUNTERS
  . A ROM WHERE THE TV STANDARD TIMING FEATURES ARE STORED
  . CONTROL LOGIC DELIVERING SIGNALS TO THE CONTROLER AND THE DECODER.

2.2.1. DOT FREQUENCY

- THE PICTURE DOT FREQUENCY IS GENERATED BY AN OSCILLATOR THE INDUCTANCE OF WHICH IS CONNECTED TO THE CIRCUIT PINS OBE AND OBS. THE OSCILLATOR IS FREE-RUNNING IN THE ANTIOPE MODE BUT IN THE NORMAL TV PICTURE MODE (INSERTION OR SUPER-IMPOSITION) THE OSCILLATOR IS RESYNCHRONISED BY THE SYNC LINE PULSES APPLIED TO PIN SLL.

2.2.2. COUNTERS AND ROM

- THE CHARACTER, LINE AND FRAME COUNTERS ASSOCIATED WITH SEQUENCING LOGIC WHICH PRESETS EACH COUNTER FROM A MASK PROGRAMMABLE ROM PROVIDE THE FOLLOWING FEATURES :

  . ADAPTABILITY TO THE TIMING CHARACTERISTICS OF ANY TV STANDARD
  . ADJUSTMENT OF THE DISPLAY AREA IN X AND Y DIRECTIONS IS POSSIBLE
  . CHOICE OF THE NUMBER OF ROWS AND THE NUMBER OF CHARACTERS PER ROW (THE NUMBER OF CHARACTERS MUST BE EVEN)
  . CHOICE OF THE NUMBER OF LINES IN THE CHARACTER MATRIX.

- THE ROM PROGRAMMATION PARAMETERS ARE DETAILLED IN APPENDIX 1.

- THE ROM CONTENTS ALLOW THE CHOICE BETWEEN TWO TYPES OF STANDARD (THE VARIOUS OPTIONS CHOSEN ARE INDICATED IN APPENDIX 1), AND BIT BT2 OF THE COMMAND REGISTER CM1 OPERATES THAT CHOICE.

- THE COMMAND BIT BT1 FORCES THE FRAME MODE OF OPERATION: INTERLACING OR NON-INTERLACING.

- BIT BT3 MUST ALWAYS BE KEPT AT LOGICAL LEVEL ZERO.

2.2.3. TIME BASE SYNC LOGIC

- THE SYNC MODE OF THE TIME BASE IS SELECTED BY BIT BT4 OF THE CM1 COMMAND REGISTER AND BIT DC1 OF THE CM2 COMMAND REGISTER.

NORMAL TV PICTURE MODE: DC1 = 0

- THE FRAME SYNC AND LINE SYNC DETECTION IS NECESSARY IN THE NORMAL TV MODE IN ORDER TO PLACE THE INSERTED OR SUPERIMPOSED AREA CORRECTLY WITHIN THE ANALOG TV PICTURE.

- THE PINS SLL AND SCT ARE THE INPUT PINS FOR THE LINE AND FRAME SYNC PULSES.

COMMAND BIT BT4 = 1 :

- THE LINE SYNC IS INPUT ON PIN SLL AND THE COMPOSITE SYNC ON PIN SCT. A LOGIC ARRAY OPERATES THE DETECTION OF THE LEADING AND TRAILING EQUALIZATION PULSES WITHIN THE COMPOSITE SYNC. THE TIME BASE SEQUENCING LOGIC IS RESYNCHRONIZED AT THE END OF THE TRAILING EQUALIZATION TIME.

COMMAND BIT BT4 = 0 :

- THE LINE SYNC IS INPUT ON PIN SLL AND THE FRAME SYNC ON PIN SCT, AND THE TIME BASE SEQUENCING LOGIC IS RESYNCHRONIZED ON EACH FRAME SYNC PULSE.

NOTE : IN BOTH CASES (BT4 = 0 AND BT4 = 1) DESCRIBED ABOVE THE LINE SYNC PULSE IS USED TO SYNCHRONISE THE DOT OSCILLATOR.

ANTIOPE MODE (DC = 1)

COMMAND BIT BT4 = 0

- THE TIME BASE IS FREE RUNNING. THE LOGIC ARRAY DETECTING THE LEADING AND TRAILING EQUALIZATION PULSES REMAINS OPERATIONAL AND SETS THE ST2 STATUS BIT FROM THE SLL AND SCT INPUTS (SEE CHAPTER 2.1.1.2. AND TABLE 5)

COMMAND BIT BT4 = 1

- THE CIRCUIT PINS SLL AND SCT ARE OUTPUT PINS DELIVERING THE LINE SYNC PULSES AND THE FRAME SYNC PULSES. THE PULSE DURATIONS AND PERIODS ARE PROGRAMMED IN THE TIME BASE ROM.

SUB-TITLING

- THE COMMAND BIT BT5 = 1 SELECTS THE SUBTITLING MODE.

- THE UPPER AND LOWER BORDERS ARE THEN EXTENDED AND THE DISPLAY AREA REDUCED TO A LIMITED NUMBER OF ROWS. FOR EXAMPLE : 3 ROWS OF SUBTITLES LIMIT THE PAGE MEMORY TO 240 BYTES, THUS SMALL SIZE MEMORIES CAN BE USED FOR DISPLAY TERMINALS DEDICATED TO THIS PURPOSE (SEE APPENDIX 1).

- THE BASE ADDRESS BAPA SELECTS THIS REDUCED PAGE, WHICH IS DISPLAYED IN THE SAME WAY AS A FULL PAGE IN THE ANTIOPE MODE, BY INSERTION OR SUPERIMPOSITION.

2.2.4. CONTROL LOGIC

- THE CONTROL LOGIC DELIVERS THE VARIOUS SIGNALS NECESSARY FOR CONTROLLER AND DECODER OPERATION. THE MAIN BLOCKS OF THIS LOGIC ARE THE FOLLOWING :

  . FLASHING COUNTER
  . ADDRESSING OF THE LINE TO BE DISPLAYED FOR NORMAL AND DOUBLE HEIGHT CHARACTERS
  . GENERATION OF PAGE MEMORY ACCESS REQUEST
  . DISPLAY AREA DECODING

2.3. DECODER (FIG. 13)

- THE DECODER PRODUCES THE DOT COLOR SIGNALS USING THE DATA STORED IN THE PAGE DISPLAY MEMORY AND IN THE CHARACTER GENERATORS, TOGETHER WITH THE TIMING SIGNALS COMING FROM THE TIME BASE.

2.3.1. DATA USED BY THE DECODER

- THE DATA STORED IN THE DISPLAY REGISTER IS TRANSFERRED TO THE DECODER BY THE CONTROL CIRCUIT. THIS DATA IS READ IN TWO DIFFERENT WAYS, ACCORDING TO THE DECODER MODE : MAPPING OR VIDEOTEX

- IN VIDEOTEX MODE THE DISPLAY REGISTER CONTENT IS :

  . CHARACTER CODE 7 BITS
  . ATTRIBUTES 9 BITS
  . CHARACTER DOTS (CHARACTER LINE) 8 BITS

- IN MAPPING MODE THE DISPLAY REGISTER CONTENT CONSISTS OF 24 BITS WHICH REPRESENT THE R,G,B SIGNALS FOR AN 8 DOT DISPLAY.

- THE CONTROL CIRCUIT ALSO SENDS THE CM2 REGISTER CONTENTS TO THE DECODER AND THE TIME BASE PROVIDES THE DECODER WITH THE LINE, CHARACTER AND DOT CLOCKS, AND THE SIGNALS WHICH DEFINE THE DISPLAY AREA.

2.3.2. DECODER OPERATION

- FOR EACH CHARACTER MATRIX DOT THE DECODER PRODUCES R,G,B SIGNALS FROM

  . THE 8 DOTS OF THE MATRIX
  . THE CHARACTER ATTRIBUTES : F1 TO F9 WHICH DEFINE COLOR AND SIZE CHARACTERISTICS, AND SOME OTHER FUNCTIONS
  . THE CHARACTER CODE USED TO DELIMIT THE DISPLAYED AREA CHARACTERISTICS
  . THE BITS STORED IN CM2 COMMAND REGISTER

MAPPING MODE

- THE DISPLAY REGISTER CONTAINS THE R,G,B DOTS TO BE DISPLAYED. NO DECODING IS NEEDED, THE SIGNAL IS SENT DIRECTLY TO THE OUTPUT.

MIX MODE

- THE DECODER OPERATES USING THE TWO ABOVE MODES ALTERNATIVELY. THE SWITCH FROM ONE MODE TO THE OTHER ONE IS COMMANDED BY THE CONTROLLER.

2.3.3. DECODER COMMAND BITS (SEE TABLE 6)

DC1

- THIS BIT CHOSES BETWEEN FULL SCREEN DISPLAY ANTIOPE MODE OR TELEVISION MODE IN ORDER TO DISPLAY SUPERIMPOSED OR INSERTED DATA. THE SYNC SWITCHING C SIGNAL IS DIRECTLY RELATED TO DC1.

DC2 : ROW ZERO DISPLAY

- THIS COMMAND IS USED ONLY IN VIDEOTEX MODE (MIXED OR NOT). IF DC2 = 0, THE ROW ZERO IS DISPLAYED WITH A BORDER COLOR IDENTICAL TO THE BACKGROUND COLOR

DC3 : MASKING COMMAND

- THIS IS USED ONLY IN VIDEOTEX MODE. DC3 = 1 MASKS THE STRING DEFINED CHARACTER FIELDS, IF DC3 = 0, THEY ARE NOT MASKED.

DC4 : INSERTION COMMAND
IDEM

DC7 : UNDERLINING COMMAND
IDEM

DC5 : 4TH ALPHABET COMMAND

- USED ONLY IN VIDEOTEX MODE (THE 4TH ALPHABET MAY BE ALPHANUMERIC OR BLOCK GRAPHIC)

DC6 : GRID DISPLAY

- USED ONLY IN VIDEOTEX MODE. WHEN USED, THE LAST LINE AND THE FIRST POINT OF EACH LINE OF CHARACTER MATRIX APPEAR WITH COMPLEMENTARY COLOR

DC8 :

- THIS COMMAND ALLOWS INSERTION REPLACEMENT BY SUPERIMPOSITION.

2.3.4. SCREEN ATTRIBUTES (TABLE 7)

- CM4 CONTROL CIRCUIT REGISTER STORES SCREEN ATTRIBUTES. THEY ARE USED ONLY IN VIDEOTEX MODE.

BM, VM, RM

- THESE 3 BITS DEFINE THE COLOR OF THE BORDER SURROUNDING THE PAGE DISPLAYED ON THE SCREEN. THIS COLOR IS ALSO USED BY DEFAULT AT THE BEGINNING OF A ROW (VIDEOTEX MODE ONLY)

MR

- IS USED TO MASK THE FULL SCREEN. IN THIS CASE THE TEXT AND THE BACKGROUND COLOR ARE REPLACED BY THE BORDER COLOR

LR

- IS USED TO UNDERLINE ALL CHARACTERS ON THE SCREEN, WITH THE EXCEPTION OF THE SPACE CHARACTER.

IR

- IS USED TO INSERT A FULL PAGE ON THE SCREEN, INCLUDING TEXT AND BORDER.
- COMMAND BITS DC3, DC4, AND DC7 (SEE TABLE 6) RETAIN THEIR NORMAL FUNCTION AS WELL AS THE FIELD ATTRIBUTES WHICH HAVE PRIORITY OVER THE SCREEN ATTRIBUTES.
- WHEN THE VIDEOTEX MODE IS USED, THE CM4 REGISTER COMMAND BITS ARE USED AS DEFAULT OPTIONS FOR EACH ROW.

3.5. ROW ATTRIBUTES

- ROW ATTRIBUTES ONLY APPLY TO MAPPING OR MIX MODE.

- IF A PAGE CONSISTING OF ALPHANUMERIC CHARACTERS INCLUDES ONLY VIDEOTEX MODE ROWS, IT MAY BE NEVERTHELESS DISPLAYED USING THE MIX MODE. IT WILL THEN BENEFIT OF ROW ATTRIBUTES.

- IN MIX OR MAPPING MODE, THE CM4 REGISTER CONTENT IS MODIFIED AT THE END OF EACH ROW (OR LINE) BY THE CONTENT OF THE BYTE NUMBER 81 IN VIDEOTEX MODE OR BY THE CONTENT OF THE BYTE NUMBER 121 IN MAPPING MODE. THE CM4 REGISTER THEN CONTAINS AT THE BEGINNING OF EACH ROW (OR LINE) THE ATTRIBUTES (DEFINED IN PARAGRAPH 2.3.4.) WHICH WILL RETAIN THE SAME MEANING FOR THE COMPLETE ROW (OR LINE). IN MAPPING MODE, THE UNDERLINING FUNCTION DOES NOT APPLY AND THE MASKING AND INSERTION FUNCTIONS APPLY FOR A COMPLETE LINE.

- THE C/G BIT CAN ONLY BE A ROW ATTRIBUTE. IT ALLOWS SELECTION OF THE NEXT ROW (OR LINE) DISPLAY MODE (VIDEOTEX MODE IF C/G = 0, MAPPING MODE IF C/G = 1).

2.3.6. FIELD ATTRIBUTES

- THE FIELD ATTRIBUTES ARE USED ONLY IN VIDEOTEX MODE.

- A SPACE (CHARACTER CODE 20) IS USED AS A BOUNDARY FOR A FIELD ATTRIBUTE. THE MEANING OF THE ATTRIBUTES OF THIS CHARACTER IS SHOWN IN TABLE 8. THE SPACE CHARACTER IS A CHARACTER WITH ALL POINTS ACTIVE (LOGICAL 1).
- WHEN THE SPACE CHARACTER IS DECODED, F1, F5, F6, F7, F8, F9 ARE STORED UNTIL ANOTHER SPACE CHARACTER OR END OF ROW IS ENCOUNTERED.

F1

- F1 = 1 DEFINES THE BEGINNING OF AN AREA WITH INSERTION OR SUPERIMPOSITION IN THE TV PICTURE. THE END OF THIS AREA IS DEFINED BY F1 = 0 OR THE END OF THE ROW. THE SPACE CHARACTER (ALL ZERO CHARACTER) IS INSIDE THE INSERTED (OR SUPERIMPOSED) AREA. THE AREA APPEARS ON THE SCREEN WHEN DC4 = 1

F2, F3, F4

- DEFINE THE SPACE COLOR

F5

- F5 = 1 DEFINES THE BEGINNING OF AN UNDERLINED AREA. F5 = 0 OR THE END OF THE ROW DEFINES THE END OF AN UNDERLINED AREA. THE SPACE CHARACTER IS NOT UNDERLINED. THE AREAS APPEAR ON THE SCREEN WHEN DC7 = 1.

F6

- F6 = 1 DEFINES THE BEGINNING OF A MASKED AREA. F6 = 0 OR THE END OF THE ROW DEFINES THE END OF THE MASKED AREA. WHEN DC3 = 1, THE MASKED AREA IS DISPLAYED AS A SPACE WITH THE COLOR OF THE BACKGROUND OF THE FIRST CHARACTER PRECEDING THE AREA CHARACTER BOUNDARY.

F7, F8, F9

- THESE BITS DEFINE THE FOLLOWING AREA BACKGROUND COLOR. THIS COLOR IS USED UNTIL ANOTHER SPACE CHARACTER IS FOUND OR UNTIL THE END OF THE ROW. WITH A BLOCK GRAPHIC CHARACTER, THESE BITS HAVE THE SAME MEANING.

2.3.7. CHARACTER ATTRIBUTES (TABLES 9.1 AND 9.2)

- THE CHARACTER ATTRIBUTES ARE SENT WITH EACH CHARACTER TO BE DISPLAYED (VIDEOTEX MODE ONLY).

- THE F1 AND F6 BITS ARE USED TO SELECT ONE OUT OF FOUR DIFFERENT CHARACTER GENERATORS.

F1, F6

- THE F1 AND F6 BITS ALLOW SELECTION OF ONE OF THE FOUR CHARACTER GENERATORS ASSOCIATED WITH A PAGE TO BE DISPLAYED. F1 AND F6 SELECT ONE OF THE FOUR BASE ADDRESSES BAGC0 TO BAGC3.

F2, F3, F4

- THESE 3 BITS DEFINE THE COLOR OF THE DOTS REPRESENTED BY A LOGICAL ONE IN THE ALPHANUMERIC OR BLOCK GRAPHIC CHARACTER MATRIX.

F5

- THIS BIT ALLOWS THE FLASHING OF ONE CHARACTER. DURING 32 FRAMES OUT OF 64 ALL DOTS OF THE CHARACTER MATRIX ARE FORCED TO ZERO. BY THIS WAY THE CHARACTER IS ALTERNATIVELY DISPLAYED WITH ITS COLOR AND WITH THE BACKGROUND COLOR.

F7, F8, F9

- IF F1, F6 AND DC5 ARE DEFINING A BLOCK GRAPHIC CHARACTER, THESE 3 BITS DEFINE THE BACKGROUND DOT COLOR (THE BACKGROUND DOTS ARE DEPICTED BY A LOGICAL ZERO IN THE CHARACTER MATRIX).

- THESE BITS ALSO DEFINE THE NEXT CHARACTER BACKGROUND COLOR IF THEY ARE ALPHANUMERIC.

BOUNDARY,

- IF THE CHARACTER IS ALPHANUMERIC THE BITS F7, F8, F9 RESPECTIVELY DEFINE DOUBLE HEIGHT, DOUBLE WIDTH AND REVERSED BACKGROUND.

F7 : DOUBLE HEIGHT

- THE DOUBLE HEIGHT IS OBTAINED BY ADDRESSING TWICE THE SAME FIGURE OF THE CHARACTER MATRIX. TO GET GOOD CHARACTER ALIGNMENT OF SIMPLE AND DOUBLE HEIGHT CHARACTERS, THE MATRIX UPPER LINE IS READ 3 TIMES, WHEREAS THE LAST LINE IS READ ONLY ONCE.

F8 : DOUBLE WIDTH

- THE DOUBLE WIDTH IS OBTAINED BY DOUBLING THE WIDTH OF EACH DOT OF THE MATRIX. THE DOUBLE WIDTH AND DOUBLE HEIGHT CODES MUST BE DUPLICATED IN THE PAGE MEMORY : WITH DOUBLE HEIGHT THEY MUST BE DUPLICATED IN THE TWO CONSECUTIVE ROWS, AND WITH DOUBLE WIDTH THEY MUST BE DUPLICATED IN THE TWO CONSECUTIVE CHARACTERS.

F9 : REVERSED BACKGROUND

- THIS ATTRIBUTE COMMANDS THE EXCHANGE OF THE CHARACTER AND BACKGROUND COLORS.

NOTE

- THE UNDERLINING COMMAND SUBDIVIDES THE BLOCK GRAPHICS CHARACTERS : LINES 2, 6 AND 9 AS WELL AS COLUMNS NBR. 0 AND 4 ARE DISPLAYED WITH THE COLOR DEFINED FOR THE BACKGROUND.

2.3.8. I OUTPUT MODULATION

- IN ANTIOPE MODE DC1 = 1, THE I SIGNAL IS ALWAYS AT LOGICAL LEVEL 1; THIS SIGNAL IS USED TO SWITCH THE VDP R, G, B OUTPUTS ON TO THE TV SET.

- IN TV MODE DC1 = 0, THE I = 0 OUTPUT SWITCHES ON THE TV SCREEN THE NORMAL ANALOG PICTURE. DURING AN INSERTION THE I OUTPUT IS SET TO LOGICAL LEVEL "1".

- DURING LINES WHICH ARE DISPLAYED IN MAPPING MODE, THE I OUTPUT CAN BE MODIFIED BY THE BYTE NBR. 122 CONTENT (THE 121ST BYTE CONTAINS THE LINE ATTRIBUTES). EACH BIT OF THIS BYTE DEFINES AN AREA CORRESPONDING TO 1/8 OF THE LINE. WHEN DC1 = 0, THIS BYTE CONTENT IS TRANSMITTED IN SERIES ON I OUTPUT AT 1/5 OF THE CHARACTER CLOCK RATE. WHEN DC1 = 1, THE BYTE IS COMPLEMENTED AND TRANSMITTED IN THE SAME WAY.

- WHEN USED WITH AN APPROPRIATE INTERFACE, THIS FEATURE CAN BE USED TO DISPLAY AREAS WITH A GREY SCALE, INSIDE A GRAPHIC PICTURE IN ANTIOPE MODE OR INSERTED IN AN ANALOG PICTURE.

2.3.9. PAGE AND ROW ATTRIBUTES OPERATION MODE

- ROW ATTRIBUTES ARE STORED IN THE BYTE NBR. 81 OF A ROW OR IN THE BYTE NBR. 121 OF A GRAPHIC ATTRIBUTE. WHEN OPERATING IN PURE VIDEOTEX MODE, THESE ATTRIBUTES ARE STORED FOR THE WHOLE PAGE IN THE CM4 REGISTER, SINCE EACH ROW HAS ONLY 80 BYTES INSTEAD OF 82. THE FIGURES DESCRIBING THE DISPLAY MODE/ATTRIBUTES RELATIONSHIP ARE VALID FOR EACH ROW IN MIXED MODE, AND FOR THE WHOLE PAGE IN VIDEOTEX MODE.

2.3.9.1. MASKING

- THE ATTRIBUTES USED ARE :

  . DC3 — ALLOWS AREA MASKING
  . MR — ALLOWS ROW MASKING
  . F6 — MASKED AREA BOUNDARY

- FIGURE 14 SHOWS THE DIFFERENT DISPLAY MODES. CASES 1 TO 6 APPLY TO VIDEOTEX MODE, CASES 1 AND 2 ALSO APPLY TO MAPPING MODE.

2.3.9.2. UNDERLINING

- ATTRIBUTES USED :

  . DC7 — AREA UNDERLINING ENABLE
  . LR — ROW UNDERLINING ENABLE
  . F5 — UNDERLINED AREA BOUNDARY

- FIGURE 15 SHOWS THE DIFFERENT UNDERLINING MODES.

- UNDERLINING IS NOT USED IN MAPPING MODE.

- THE UNDERLINING IS DISPLAYED WITH THE COLOR OF THE CHARACTER, ON MATRIX LINE 9. DOUBLE HEIGHT CHARACTERS ARE UNDERLINED AS THE NORMAL CHARACTERS. THE UNDERLINING IS NOT DOUBLED.

2.3.9.3. INSERTION AND SUPERIMPOSITION

- ATTRIBUTES USED :

  . DC4 — AREA INSERTION ENABLE
  . DC8 — SUPERIMPOSITION
  . IR — ROW INSERTION ENABLE
  . F1 — INSERTED OR SUPERIMPOSED AREA BOUNDARY

- FIGURE 16 SHOWS THE DIFFERENT MODES OF INSERTION AND SUPERIMPOSITION.

- THE DC8 COMMAND ALLOWS TO REPLACE THE BACKGROUND OF INSERTED AREA BY THE NORMAL VIDEO PICTURE.

- THE 8 CASES APPLY TO VIDEOTEX MODE, CASES 1 AND 2 APPLY ALSO TO MAPPING MODE.

TABLE 1

E1	E2	FUNCTION
1	1	INACTIVE
0	1	READ/WRITE VDP REGISTERS
0	0	READ MEMORY (DMA)
1	0	WRITE TO MEMORY (DMA)

TABLE 3

STATUS BIT	MEANING (AT LOGICAL ONE LEVEL)
ST1	NOT USED
ST2	FRAME SYNCH.
ST3	VERTICAL DISPLAY INTERVAL
ST4	READ IN ERROR
ST5	MEMORY ACCESS ENABLE
ST6	HORIZONTAL DISPLAY INTERVAL
ST7	BUFFER MEMORY OVERFLOW
ST8	BUFFER MEMORY EMPTY

TABLE 2

REGISTER	POINTER STATE (HEX.)	CONTENT	ASSIGNMENT MSB M0	M1	M2	M3	M4	M5	M6	LSB M7
POINTER	0	RETURN ADDRESS	RT8	RT4	RT2	RT1	AC8	AC4	AC2	AC1
COL	1	COLUMN ADDRESS	A8	A9	A10	A11	A12	A13	A14	A15
ROW	2	ROW ADDRESS	A0	A1	A2	A3	A4	A5	A6	A7
STAT	3	STATUS REGISTER	ST1	ST2	ST3	ST4	ST5	ST6	ST7	ST8
CM1	4	TIME BASE	BT1	BT2	BT3	BT4	BT5	X	X	X
CM2	5	DECODER	DC1	DC2	DC3	DC4	DC5	DC6	DC7	DC8
CM3	6	CONTROL UNIT	CT1	CT2	CT3	CT4	CT5	CT6	X	X
CM4	7	BORDER COLOR	BM	VM	RM	X	MR	LR	IR	X
		BASE ADDRESS :								
BAMT	8	BUFFER MEMORY								
BAMP	9	MPU								
BAPA	A	PAGE DISPLAY MEMORY								
BAGC0	B	CHAR. GEN. 0								
BAGC1	C	CHAR. GEN. 1								
BAGC2	D	CHAR. GEN. 2								
GAGC3	E	CHAR. GEN. 3								
BAMTF	F	END OF BUFFER								

CM1

TABLE 5 : TIME BASE COMMAND BITS

COMMAND	STATE	MEANING / FUNCTION
BT 1	1	FRAME INTERLACING
	0	FRAME NON-INTERLACING
BT 2		TV STANDARD SELECTION
	BT2 0	STANDARD 1)) SEE OPTION APPENDIX I
	BT2 1	STANDARD 2)
BT 3	0	NOT USED, MUST BE ZERO
BT 4		TOGETHER WITH DC1, SELECTS : (SEE TABLE 6)
	DC1 BT4	SLL/SCT STATE — FUNCTION: SLL — SCT
	0 0	INPUT — HORIZONT. SYNCH — VERTICAL SYNCH
	0 1	INPUT — HORIZONT. SYNCH — COMPOSITE SYNCH
	1 0	INPUT — HORIZONT. SYNCH — COMPOSITE SYNCH
	1 1	OUTPUT — HORIZONT. SYNCH — VERTICAL SYNCH
BT 5	1	SUB-TITLING

00 H & 50 Hz

BT 5 = 0 NOW SOUSTITRAGE

CM2

TABLE 6 : DECODER COMMAND BITS

COMMAND	STATE	FUNCTION
DC1	0	NORMAL TV PICTURE
	1	ANTIOPE
DC2	1	DISPLAY OF ROW ZERO
DC3	1	MASKING ENABLE
DC4	1	INSERTION ENABLE
DC5		ALPHABET NBR. 4 PROCESSING (F1=1, F6=1):
	1	BLOCK GRAPH. CHAR.
	0	ALPHANUM. CHARACT.
DC6	1	GRID DISPLAY
DC7	1	UNDERLINING ENABLE
DC8	1	SUPERIMPOSITION ENABLE

50 H
58 H
58
53

CM3

TABLE 4.1 : CONTROL UNIT COMMAND BITS

COMMAND BITS	STATE	MEANING/FUNCTION
CT1, CT2		COMMAND BITS USED BY DECODER AND CONTROL UNIT FUNCTION
	CT1 CT2	
	1 0	MAPPING MODE
	0 1	VIDEOTEX MODE
	1 1	MIX MODE
	0 0	NO DISPLAY
CT3	0	NOT USED, MUST BE ZERO
CT4	1	CPU ACCESS TO MEMORY DISABLED DURING DISPLAY INTERVAL (VERTICAL AND HORIZONTAL)
CT5	1	MEMORY TIMING : TYPE 1
	0	MEMORY TIMING : TYPE 2
CT6		ADDRESS FIELD SELECTION :
	0	64K/1 OR 16K/4 DRAM
	1	16K/1 DRAM

Mode code
58 H = 88 d

Mode graphique
98 H = 152 d