SECTION VII

ELECTRICAL REQUIREMENTS

This section reviews the TMS 9900 electrical requirements, including the system clock generation and interface signal characteristics. The "TMS 9900 DATA MANUAL" should be used for minimum and maximum values.

7.1 TMS 9900 Clock Generation

The TMS 9900 requires a non-overlapping four-phase clock system with high-level MOS drivers. Additional TTL outputs are typically required for external signal synchronization or for dynamic memory controllers. A single-chip clock driver, the TIM 9904, can be used to produce these clock signals. An alternative clock generator uses standard TTL logic circuits and discrete components.

The TMS 9900 requires four non-overlapping 12 V clocks. The clock frequency can vary from 2 kilohertz to 3 to 250 picofarads. The clock rise and fall times must not exceed 100 nanoseconds and must be 10 to 15 nanoseconds for higher frequencies in order to satisfy clock pulse width requirements. While the clocks must not overlap, the delay time between clocks must not exceed 50 microseconds at lower frequencies. The typical clock timing for 3 MHz is illustrated in Figure 7-1.

7.1.1 TIM 9904 Clock Generator

The TIM 9904 (SN74LS362) is a single-chip clock generator and driver for use with the TMS 9900. The TIM 9904 contains a crystal-controlled oscillator, waveshaping circuitry, a synchronizing flip-flop, and quad MOS/TTL drivers as shown in Figure 7-2.

The clock frequency is selected by either an external crystal or by an external TTL-level oscillator input. Crystal operation requires a 16X input crystal frequency since the TIM 9904 divides the input frequency for waveshaping. For 3-megahertz operation, a 48-megahertz crystal is required. The LC tank inputs permit the use of overtone crystals. The LC network values are determined by the network resonant frequency:

$$f = \frac{1}{2\pi \sqrt{LC}}$$

For less precise frequency control, a capacitor can be used instead of the crystal.

The external-oscillator input can be used instead of the crystal input. The oscillator input frequency is 4X the output frequency. A 12-megahertz input oscillator frequency is required for a 3-megahertz output

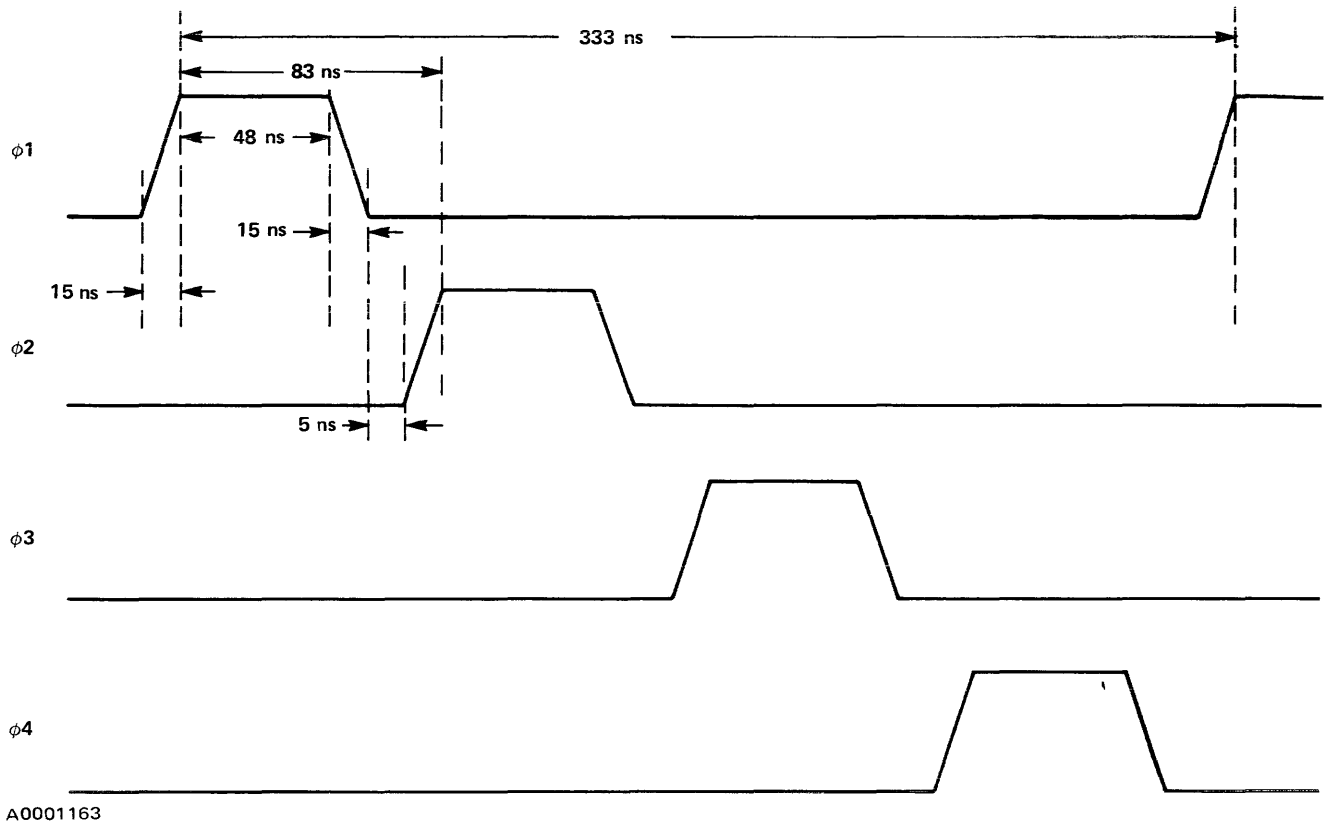

Figure 7-1. TMS 9900 Typical Clock Timing

frequency. A 4X TTL-compatible oscillator output (OSCOUT) is provided in order to permit the derivation of other system timing signals from the crystal or oscillator frequency source.

The oscillator frequency is divided by four to provide the proper frequency for each of the 4-clock phases. A high-level MOS output and an inverted TTL-compatible output is provided by each clock phase. The MOS-level clocks are used for the TMS 9900 CPU while the TTL clocks are used for system timing.

The D-type flip-flop is clocked by $\phi 3$ and can be used to synchronize external signals such as $\overline{\text{RESET}}$. The Schmitt-triggered input permits the use of an external RC network for power-on $\overline{\text{RESET}}$ generation. The RC values are dependent on the power supply rise time and should hold $\overline{\text{RESET}}$ low for at least three clock cycles after the supply voltages reach the minimum voltages.

All TIM 9904 TTL-compatible outputs have standard short circuit protection. The high-level MOS clock outputs, however, do not have short circuit protection.

7.1.2 TTL Clock Generator

Figure 7-3 illustrates an alternate TMS 9900 clock generator circuit. This system is driven by a 36 megahertz clock (minimal duty cycle restriction) which can be derived by any of several popular clock

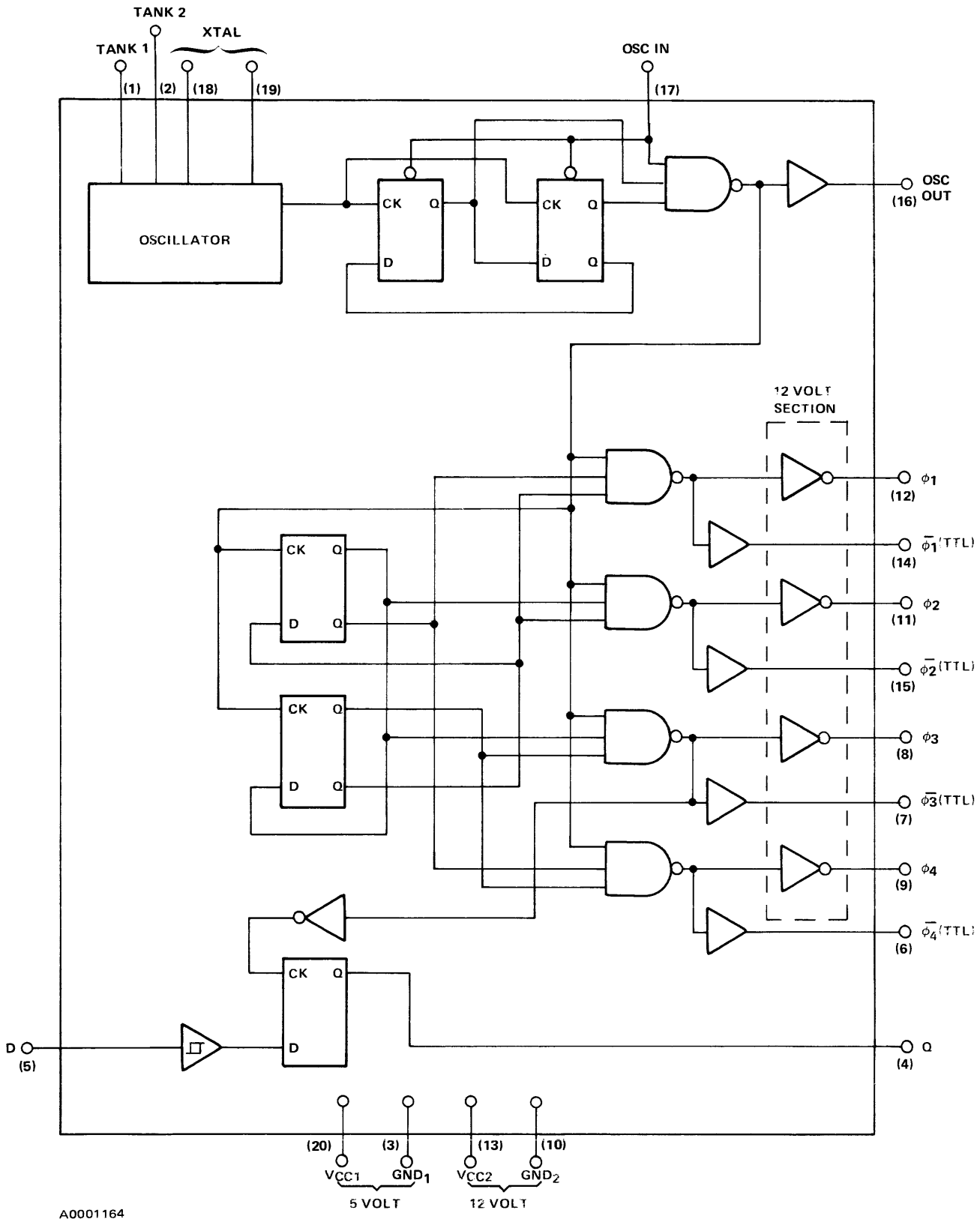

Figure 7-2. TIM 9904 Clock Generator

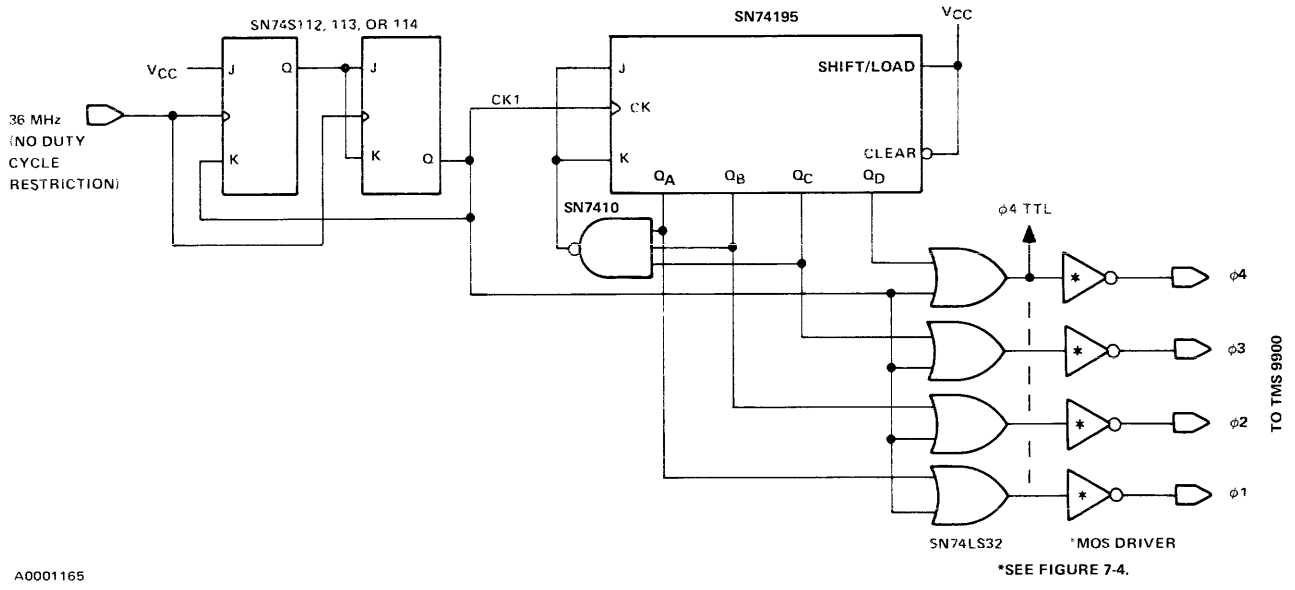

Figure 7-3. TMS 9900 Clock Generator

oscillator designs. The first stage is shown on the timing diagram in Figure 7-4 as CK1 and has a 33% duty cycle. The second stage of the generator is based on the SN74195 shift register. The shift register is connected to generate the consecutive 4-phase clocks shown for one phase as QA in the timing diagram. The shift register outputs are then gated with the input clock to form the non-overlapping TTL clocks (ϕ1TTL).

The non-overlapping TTL clocks can be translated to 12 V MOS levels by several methods. Integrated memory drivers such as the SN75355 or SN75365 can be used but may force operation at reduced frequency due to supply, temperature, or device variation.

The discrete-transistor driver shown in Figure 7-5 has been designed to allow operation at 3 megahertz over standard commercial temperature and voltage ranges.

This driver uses inexpensive 2N3703s and 2N3704s and broad tolerance passive components. Resistor tolerances can be 10% with capacitor variations as much as 20% without affecting its performance noticeably. It shows very little sensitivity to transistor variations and its propagation times are largely unaffected by output capacitive loading. It produces rise times in the 10–12 ns region with fall times from 8–10 ns, driving 200 pF capacitive loads. Propagation times for this driver are such that it produces an output pulse that is wider than its input pulse. This driver can easily be used at 3 megahertz without special selection of components. It does have the advantage of taking nine discrete components per driver, but if assembly costs are prohibitive, these can be reduced by using two Q2T2222 and two Q2T2905 transistor packs. The Q2T2222 is basically four NPN transistors of the 2N2222 type while the Q2T2905 has four PNP, 2N2905 type transistors in single 14-pin dual-in-line packages. Thus, all four drivers can be built using two packages each of these quad packs.

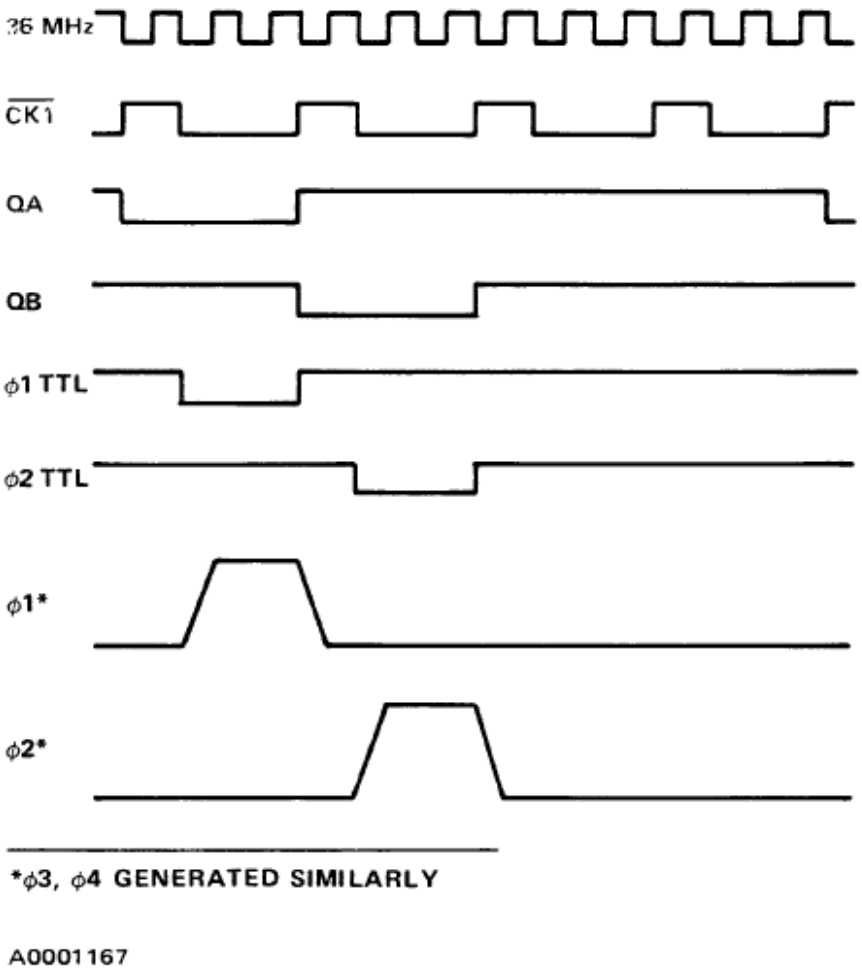

Figure 7-4. Timing Diagram for TMS 9900 Clock Generator